REMARKS

Claims 1-20 are currently pending. Claims 1-9, 11, 13-16, 19, and 20 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Barroso et al. (U.S. Pub. No. 2002/0046324, hereinafter "Barroso") in view of Zizzo (U.S. Pat. No. 6,578,174, hereinafter "Zizzo"). Claims 12 and 18 have been rejected as being unpatentable over the combination of Barroso and Zizzo in further view of Watanabe et al. (U.S. Pat. No. 6,157,947, hereinafter "Watanabe"). Applicant appreciates the indication that claims 10 and 17 are allowable, and requests reconsideration of claims 1-9, 11-16, and 18-20.

Claims 14-17 have been amended to correct typographical errors in the identified dependency of the claims.

Claims 1-9, 11, 13-16, 19, and 20 stand rejected under 35 U.S.C. §103 as being unpatentable over the combination of Barroso and Zizzo. Applicant traverses these rejections on the grounds that these references are defective in establishing a prima facie case of obviousness.

As the PTO recognizes in MPEP § 2142, 2143:

> ... The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness...
>
> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

It is submitted that, in the present case, the examiner has not factually supported a prima facie case of obviousness as, even when combined, the reference do not teach that being claimed.

Barroso discloses "[a] chip-multiprocessing system with scalable architecture, including on a single chip..." Abstract, emphasis added. Barroso teaches that the "single chip" includes multiple central processing units (CPU) and multiple data cache modules. See FIG. 1. "These first-level caches interface to other modules through the IntraChip Switch (ICS) 122. On the other side of the ICS 122 is a logically shared second level cache (L2) 130 that is interleaved into

eight separate modules, each with its own controller, on-chip tag, and data storage." Para. [0037]. Barroso further discloses that "two protocol engines, the Home Engine (HE) 140 and the Remote Engine (RE) 141, which support shared memory access multiple PIRANHA chips" are also connected to the ICS 122. Id. According to Barroso, the aforedescribed chip design, together with other features described in the patent, "realizes a far-reaching approach to chip multi-processing (CMP) by integrating eight simple processor cores along with a complete cache hierarchy, memory controllers, coherence software, and network router all onto a single chip to be built with the next generation 0.18 um CMOS process." Para. [0128]. According to the Examiner, the single chip proposed by Barroso discloses that recited in claims 1, 13, and 19 save for "generating a combination datasheet comprising a plurality of memory instances." OFFICE ACTION, July 27, 2006, p. 3.

As such, the Examiner combined Barroso with Zizzo. Zizzo discloses "[a] multi-faceted circuit design platform [that] facilitates the design of circuits and chips by making it easier for designers to locate and incorporate available virtual component blocks into new designs." Abstract. More particularly, Zizzo proposes "method and systems for facilitating electronic circuit and chip design using resources available over a distributed electronic network such as the Internet." Col. 1, lns. 8-12. Thus, one reference discloses the architecture for a single chip and another reference teaches a circuit design tool. One skilled in the art would not be motivated to combine these references. That is, Barroso teaches a scalable architecture for a single chip. Zizzo teaches a method and system for using the Internet for designing a circuit. Thus, Barroso already provides a circuit design and, at best, Zizzo teaches a system to design a circuit. Neither Barroso nor Zizzo teach or suggest re-designing of the circuit disclosed by Barroso, therefore, one skilled in the art would not be motivated to redesign Barroso's circuit using the distributed network disclosed by Zizzo.

In addition to lacking the requisite motivation to combine, neither reference, taken singly or in combination, teaches or suggests that recited in the pending claims. For example, neither reference teaches or suggests "a multi-compiler interface" or remotely linking to a selected memory compiler unit or generating a combination datasheet of a plurality of memory instances. Claim 1, for example, calls for, in part, "remotely linking to the selected first memory compiler unit (of a plurality of memory compiler units) and generating a combination datasheet comprising a plurality of memory instances." These and other elements in claims 1-20 are not

disclosed in or suggested by the art of record. Thus, the combination of the references fail to teach or suggest each and every limitation called for in the pending claims.

Accordingly, the Examiner has failed to factually establish a prima facie case of obviousness based on Barroso and Zizzo. As such, withdrawal of the rejection of claims 1-9, 11, 13-16, 19, and 20 is requested.

Claims 12 and 18 were rejected based on Barroso and Zizzo in further view of Watanabe. While Applicant disagrees with the Examiner's application of Watanabe, as set forth above, the combination of Barroso and Zizzo, even assuming the requite motivation for such a combination is present (which Applicant believes is not), fail to teach or suggest that which has been purported by the Examiner. Moreover, claims 12 and 18 are in condition for allowance as being dependent upon an otherwise allowable claim.

In conclusion, in light of at least the foregoing, claims 1-20 are believed to be in condition for allowance. A timely issuance of a Notice of Allowance for claims 1-20 is respectfully requested.

Please grant any extension of time required to enter this Amendment and charge any additional required fees to Deposit Account No. 08-1394.

Respectfully submitted,

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I hereby certify that this correspondence is being filed with the U.S. Patent and Trademark Office via EFS-Web on September 8, 2006.

Diane Sutton